# Digital Logic.
# Ways of controlling digital circuits.

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Computers use the binary number system

Only two numbers - A Zero & A One

A Voltage represents a number

+5 Volts = 1 0 Volts = 0

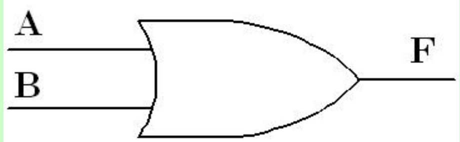
Digital logic is basically nothing more than a set of switches we use to control the flow of electricity.

## AND Gate


### Truth Table

| A | B | F |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

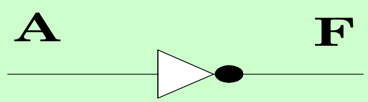
## OR Gate




### Truth Table

| A | B | F |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

## NOT Gate




### Truth Table

| A | F |
|---|---|
| 0 | 1 |
| 1 | 0 |

# Other Logic Gates

**The theorem of completeness states that OR and NOT or AND and NOT are sufficient to express all Boolean expressions.**

**We will learn here:**

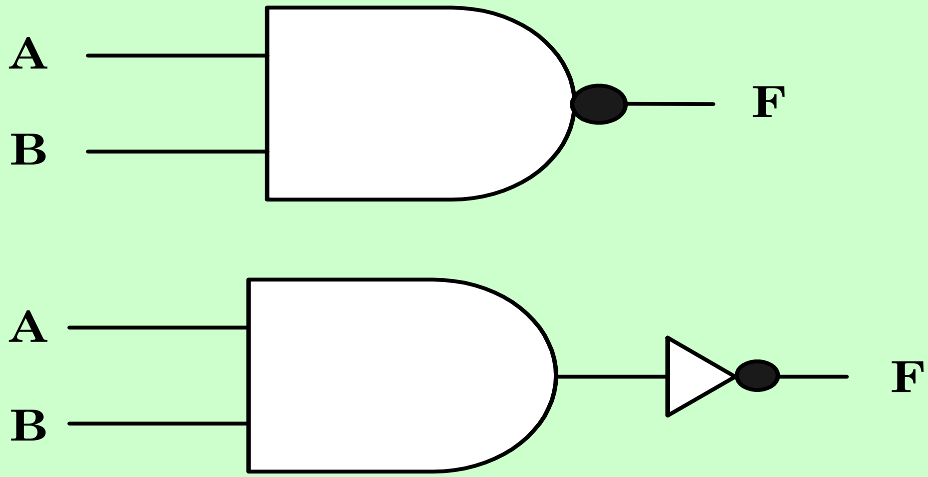
**-How to find the truth table of a digital circuit;**

**-How to analyze the scheme in order to simplify our work;**

**-How to transfer big Hex Decimal numbers using a bus with small number of wires.**

**The main idea is presented by the two to four and/or 4 to 16 decoder, the Theorem which states that every positive integer is a sum of powers of two.**

# NAND Gate




## Truth Table

AND Gate

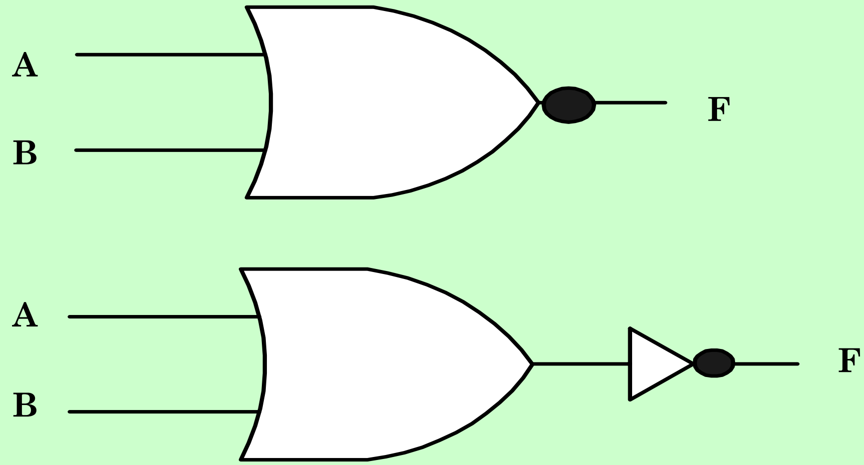
| A | B | F |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

## Truth Table

NAND Gate

| A | B | F |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

# NOR Gate




## Truth Table

OR Gate

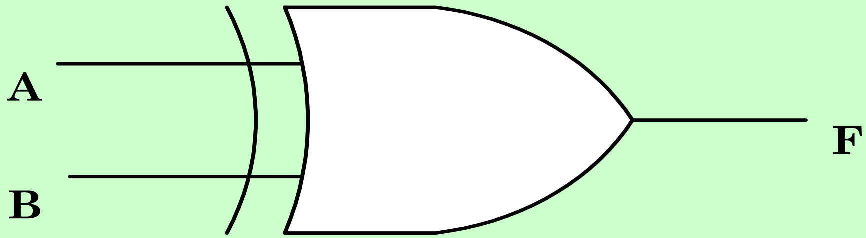
| A | B | F |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

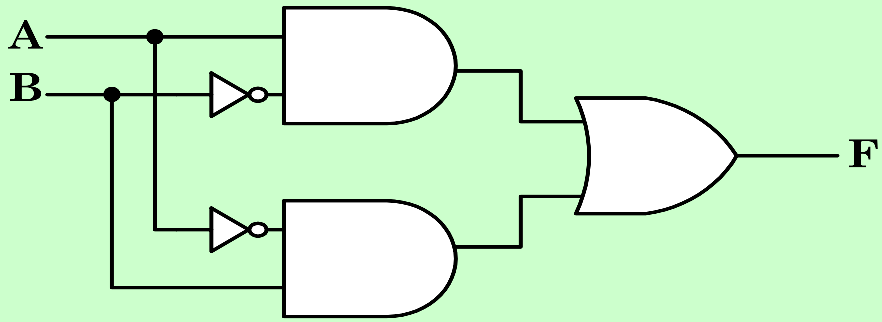
## Truth Table

NOR Gate

| A | B | F |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

**XOR (Exclusive OR)**

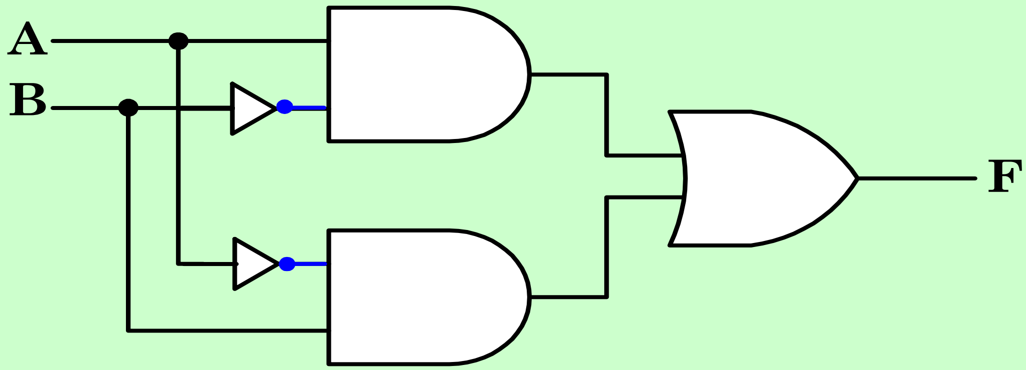



## Truth Table

| A | B | F |
|---|---|---|
| 0 | 0 | |
| 0 | 1 | |
| 1 | 0 | |
| 1 | 1 | |

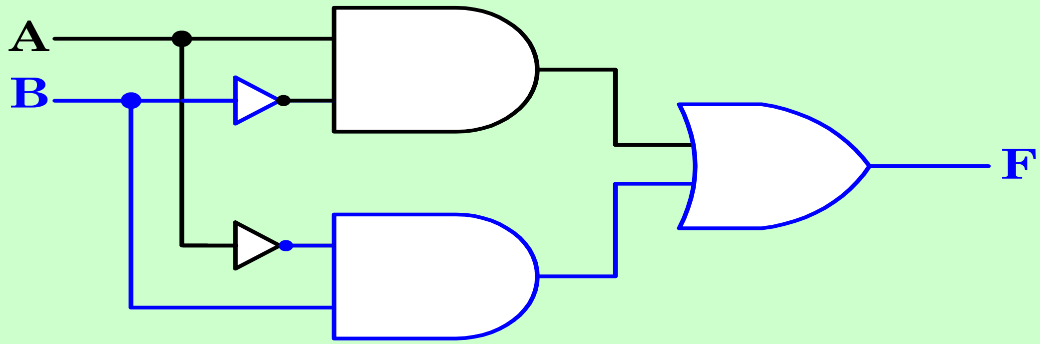
# Truth Table for XOR Gate




## Truth Table

| A | B | F |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | |
| 1 | 0 | |
| 1 | 1 | |

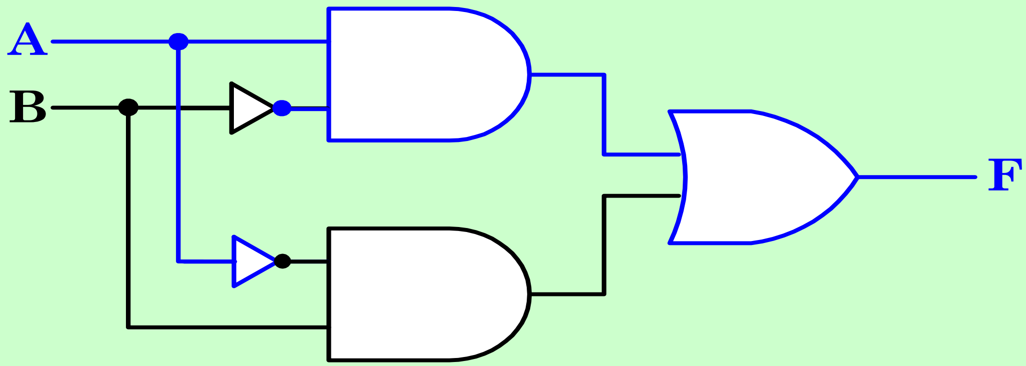
# Truth Table for XOR Gate




## Truth Table

| A | B | F |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | |
| 1 | 1 | |

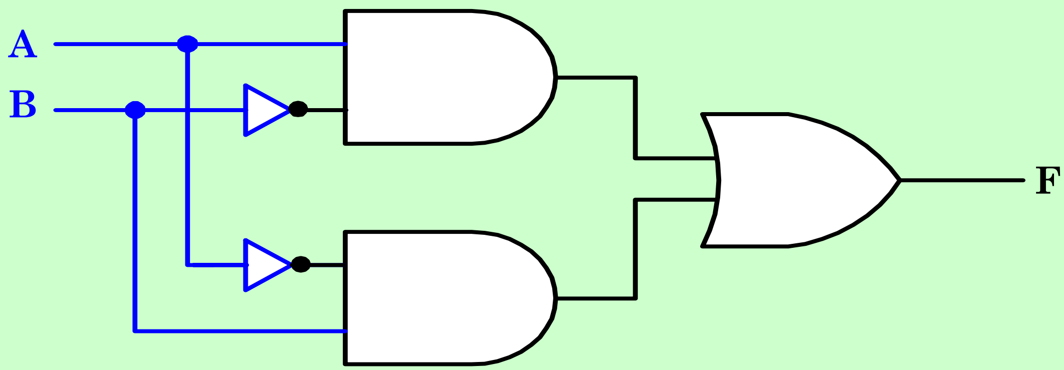
# Truth Table for XOR Gate




## Truth Table

| A | B | F |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | |

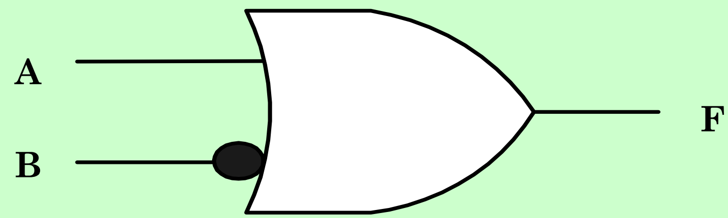
# Truth Table for XOR Gate

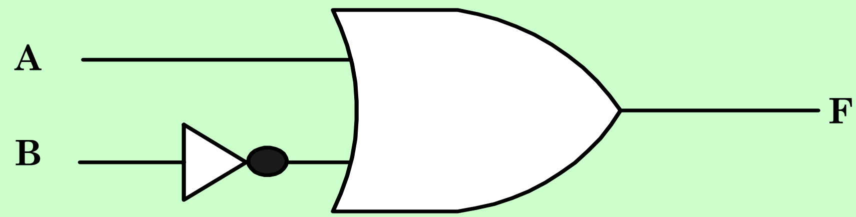



## Truth Table

| A | B | F |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

# Other Gates with NOT Gates




**Truth Table**

OR Gate

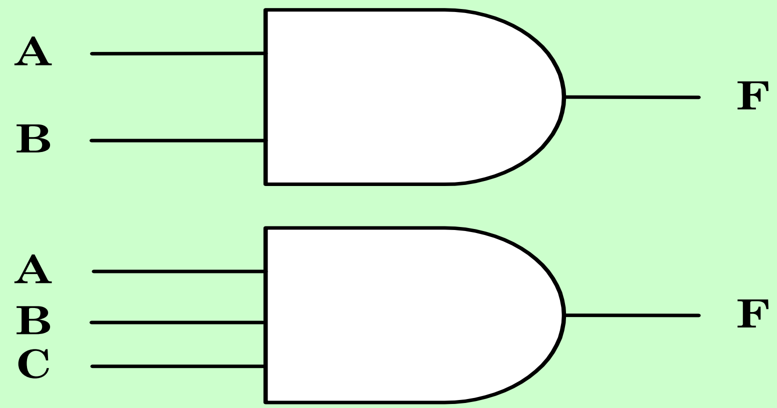
| A | B | F |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

**Truth Table**

... Gate

| A | B | F |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

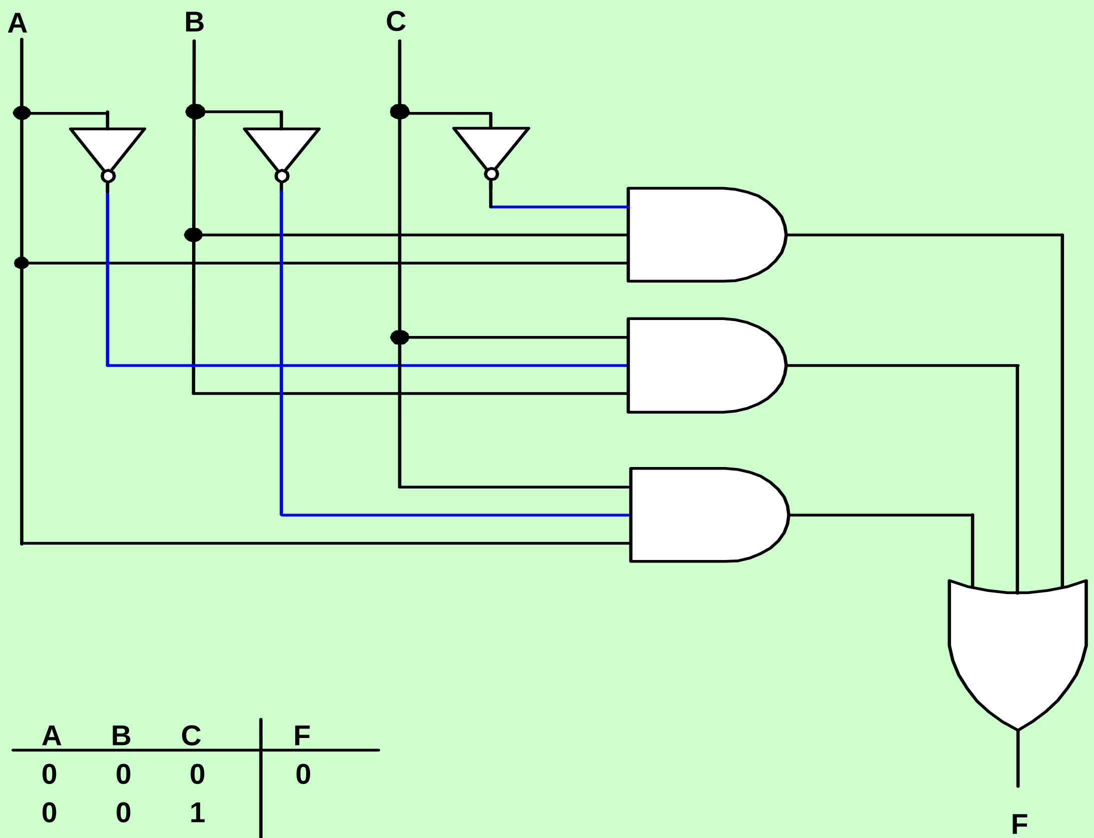
## Multi-Input Gates



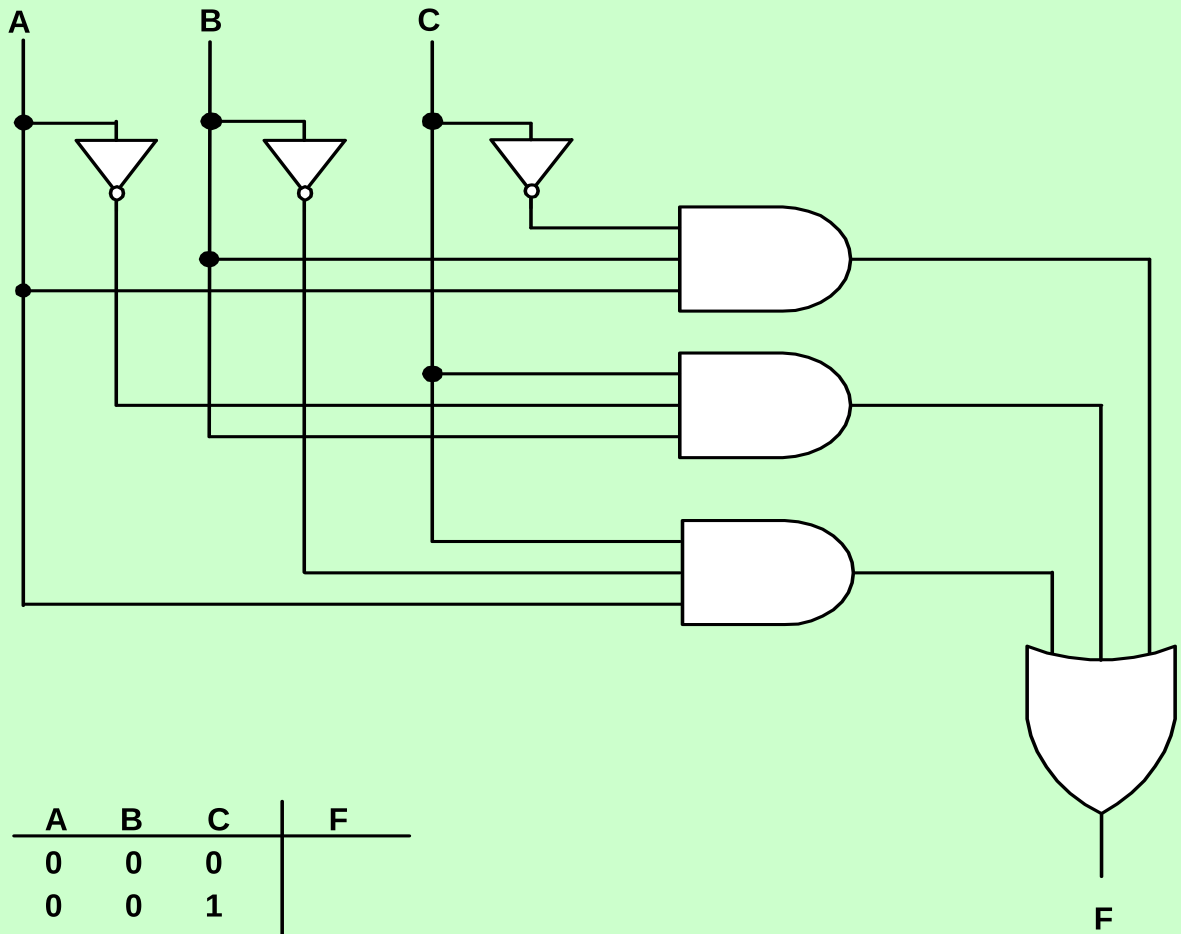

### Truth Table

**3 Input AND Gate**

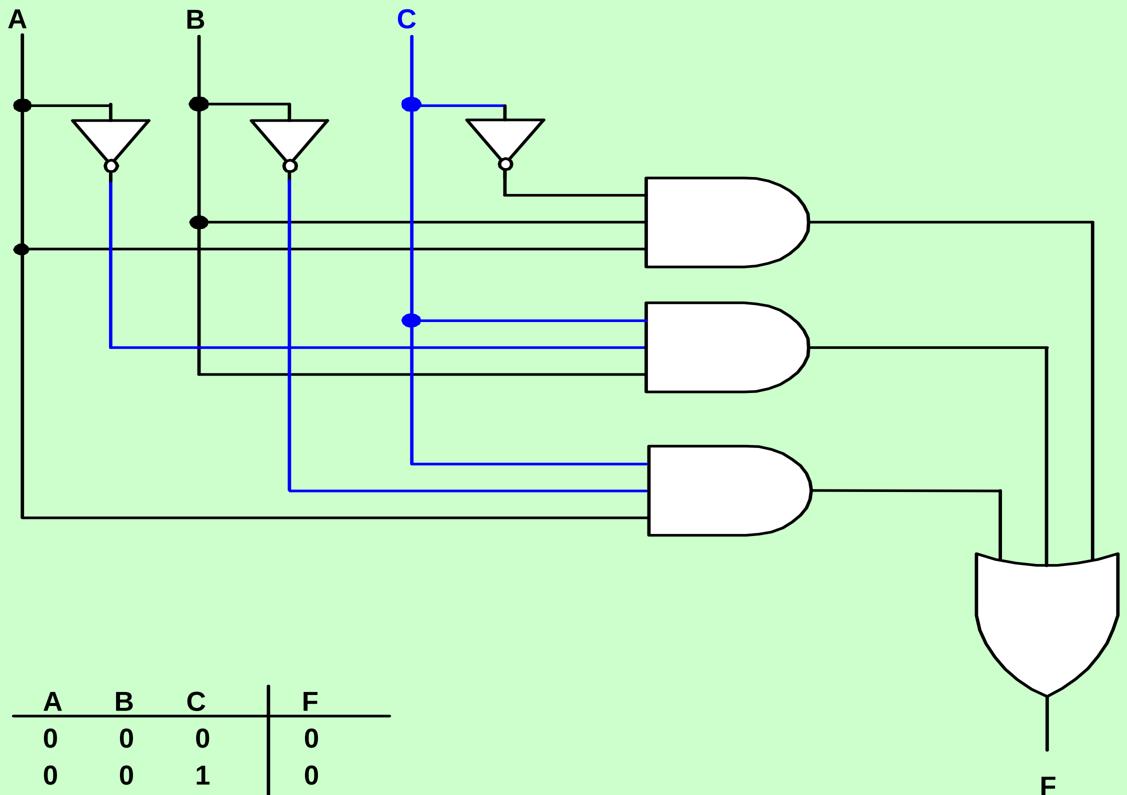
| A | B | C | F |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |



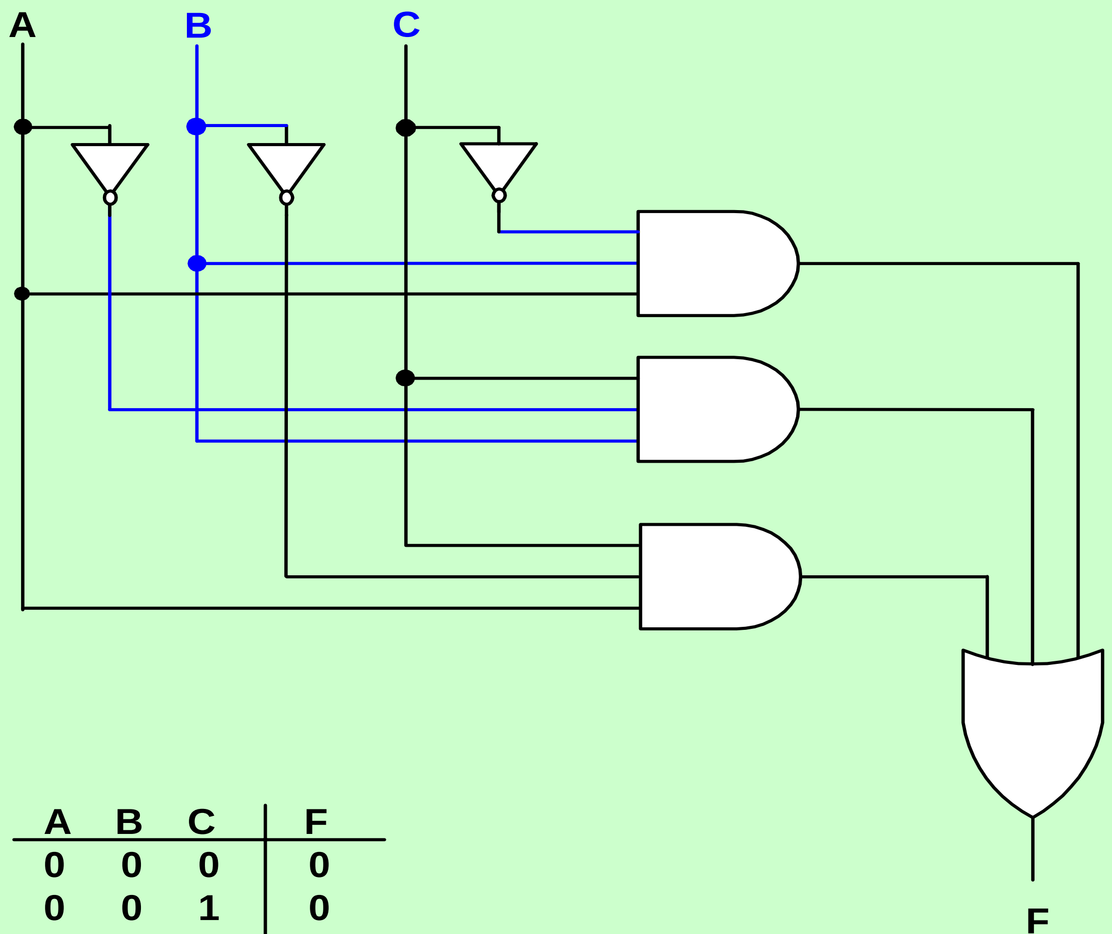

| A | B | C | F |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | |
| 0 | 1 | 0 | |
| 0 | 1 | 1 | |
| 1 | 0 | 0 | |
| 1 | 0 | 1 | |
| 1 | 1 | 0 | |
| 1 | 1 | 1 | |



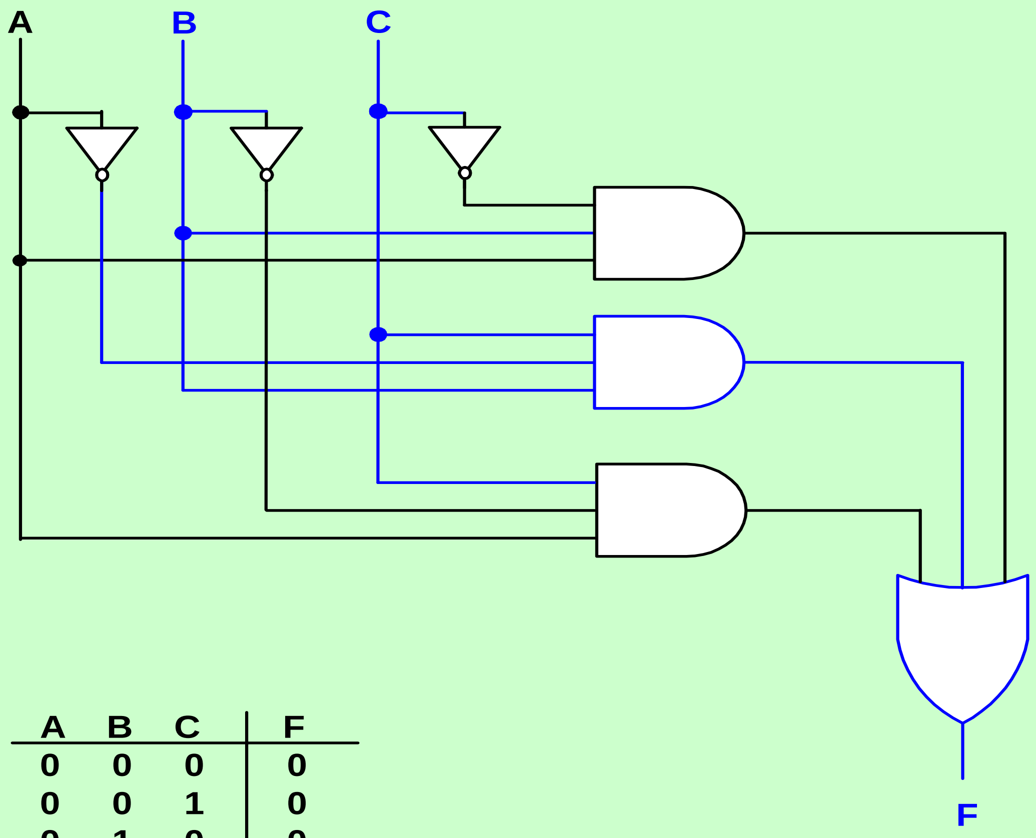

| A | B | C | F |
|---|---|---|---|
| 0 | 0 | 0 | |
| 0 | 0 | 1 | |
| 0 | 1 | 0 | |
| 0 | 1 | 1 | |
| 1 | 0 | 0 | |
| 1 | 0 | 1 | |
| 1 | 1 | 0 | |
| 1 | 1 | 1 | |



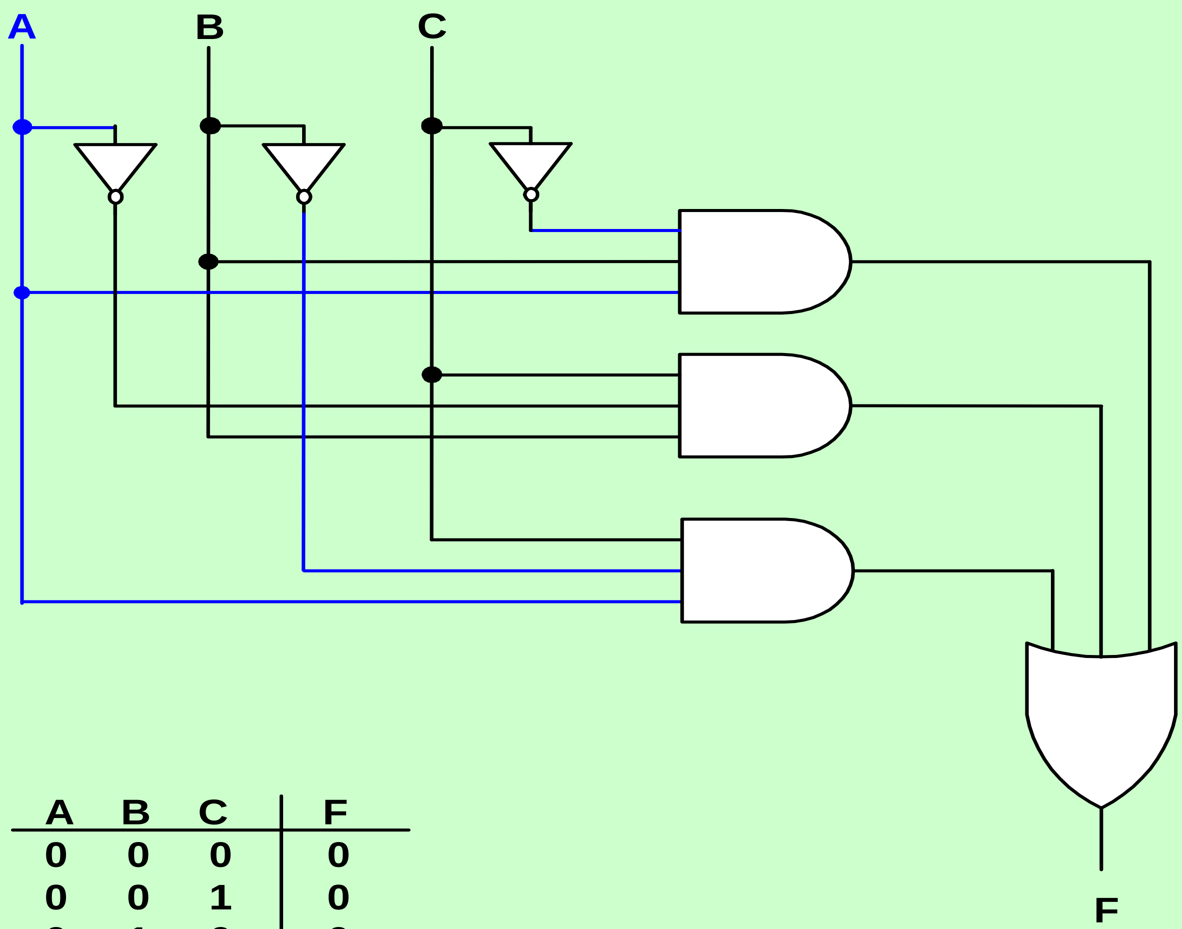

| A | B | C | F |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | |
| 0 | 1 | 1 | |
| 1 | 0 | 0 | |
| 1 | 0 | 1 | |
| 1 | 1 | 0 | |
| 1 | 1 | 1 | |



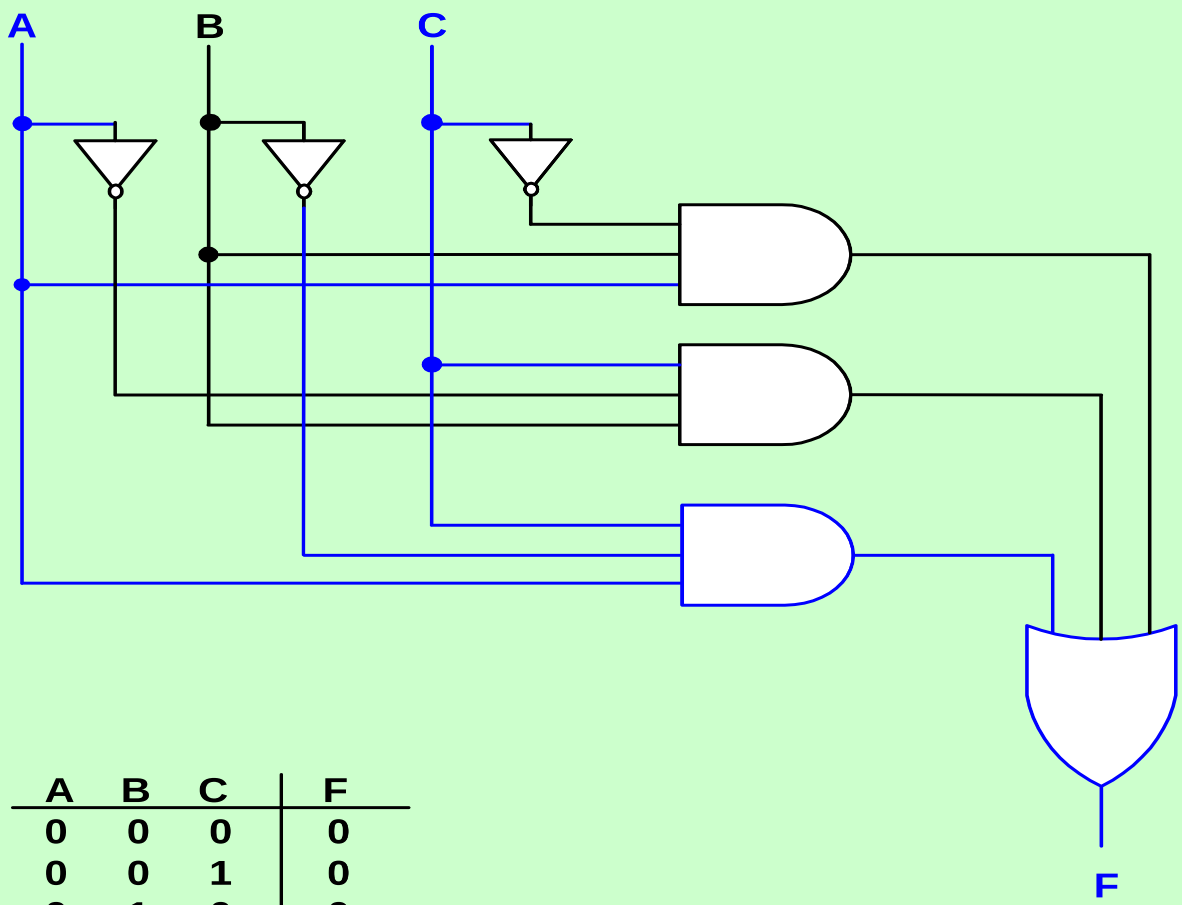

| A | B | C | F |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | |
| 1 | 0 | 0 | |
| 1 | 0 | 1 | |
| 1 | 1 | 0 | |
| 1 | 1 | 1 | |



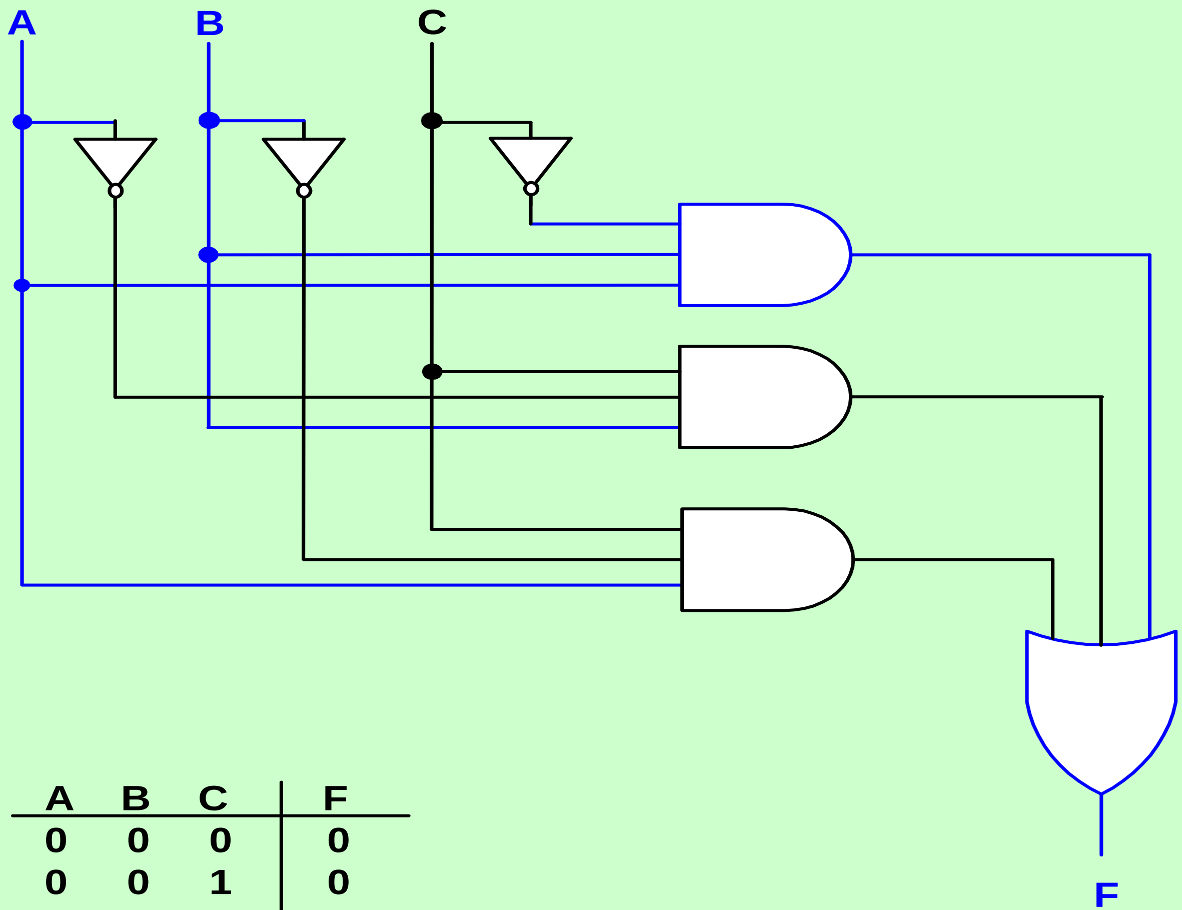

| A | B | C | F |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | |
| 1 | 0 | 1 | |
| 1 | 1 | 0 | |
| 1 | 1 | 1 | |



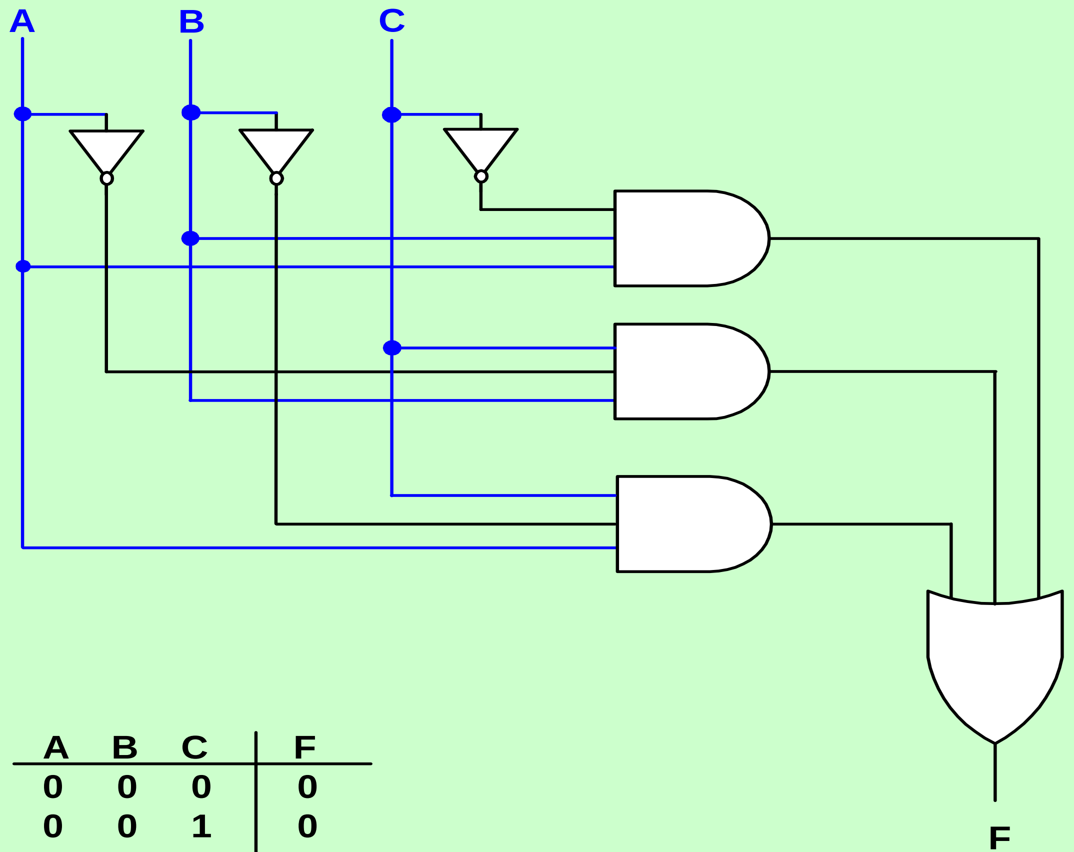

| A | B | C | F |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | |
| 1 | 1 | 0 | |
| 1 | 1 | 1 | |




| A | B | C | F |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | |
| 1 | 1 | 1 | |

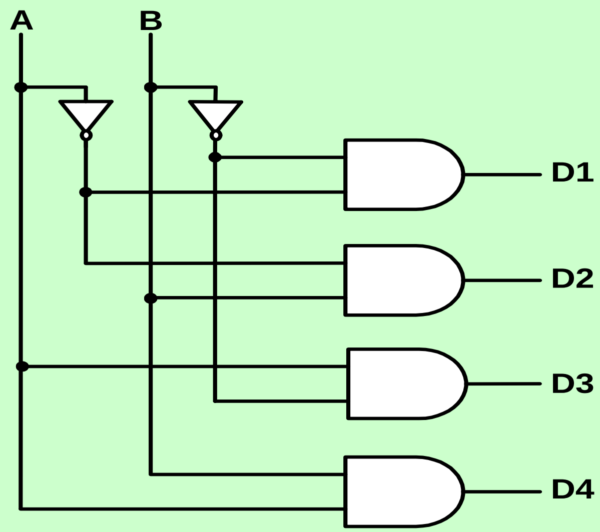



| A | B | C | F |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | |



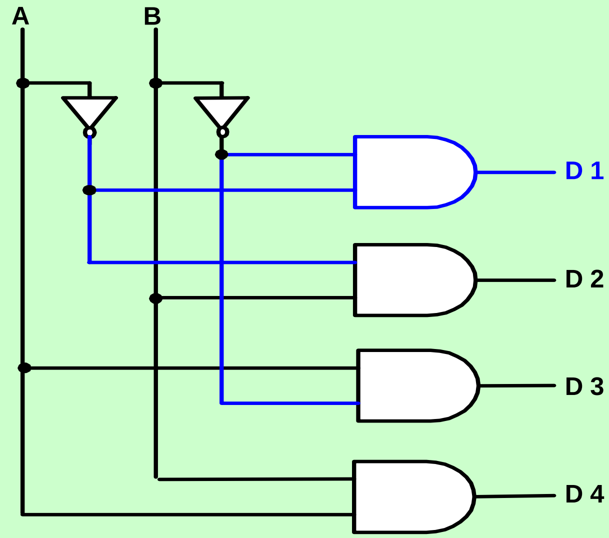

| A | B | C | F |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

# Two to Four Decode



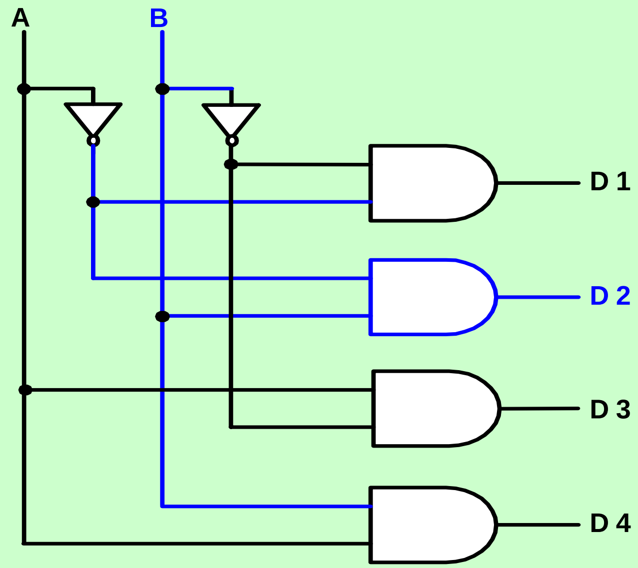

| A | B | D1 | D2 | D3 | D4 |
|---|---|---|---|---|---|
| 0 | 0 | | | | |
| 0 | 1 | | | | |
| 1 | 0 | | | | |
| 1 | 1 | | | | |

# Two to Four Decode



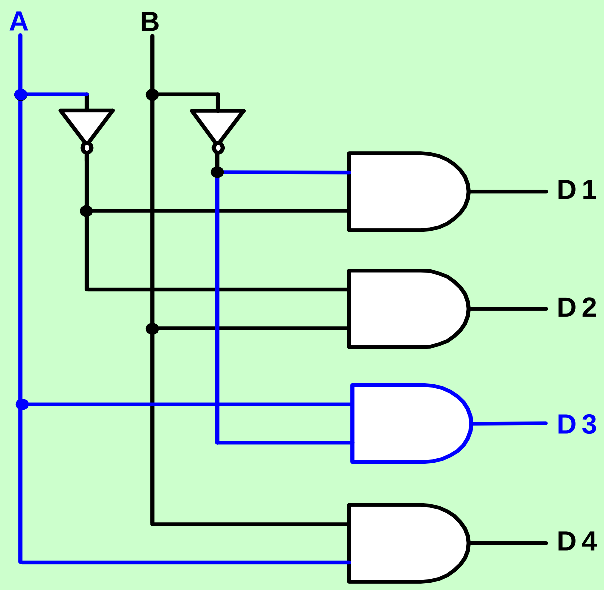

| A | B | D 1 | D 2 | D 3 | D 4 |
|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | | | | |
| 1 | 0 | | | | |
| 1 | 1 | | | | |

# Two to Four Decode



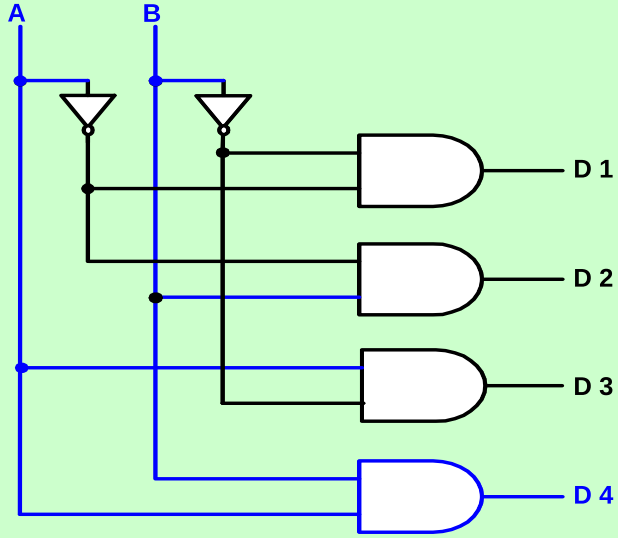

| A | B | D 1 | D 2 | D 3 | D 4 |
|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | | | | |
| 1 | 1 | | | | |

# Two to Four Decode




| A | B | D 1 | D 2 | D 3 | D 4 |
|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | | | | |

# Two to Four Decode

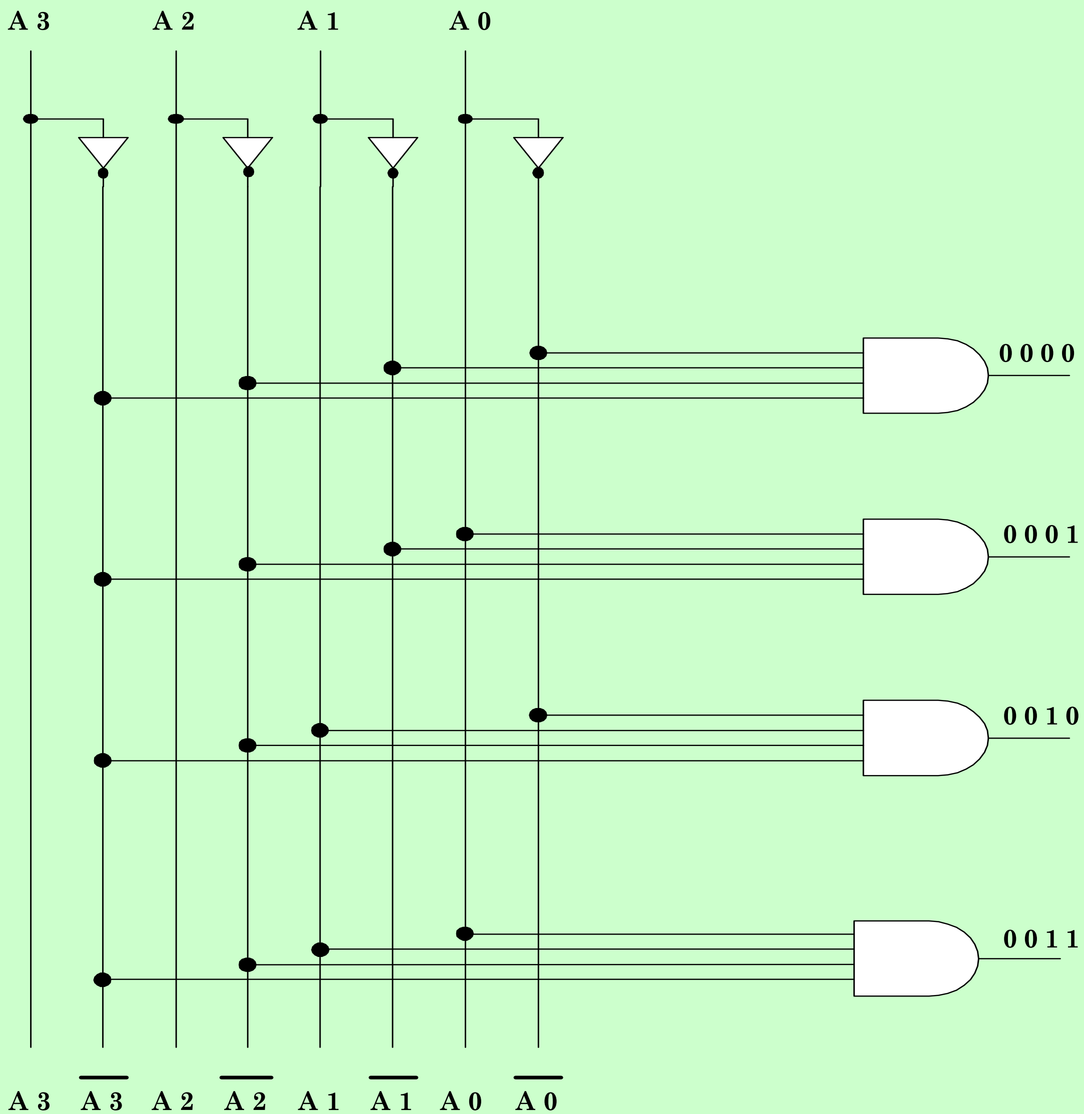



| A | B | D 1 | D 2 | D 3 | D 4 |
|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 |

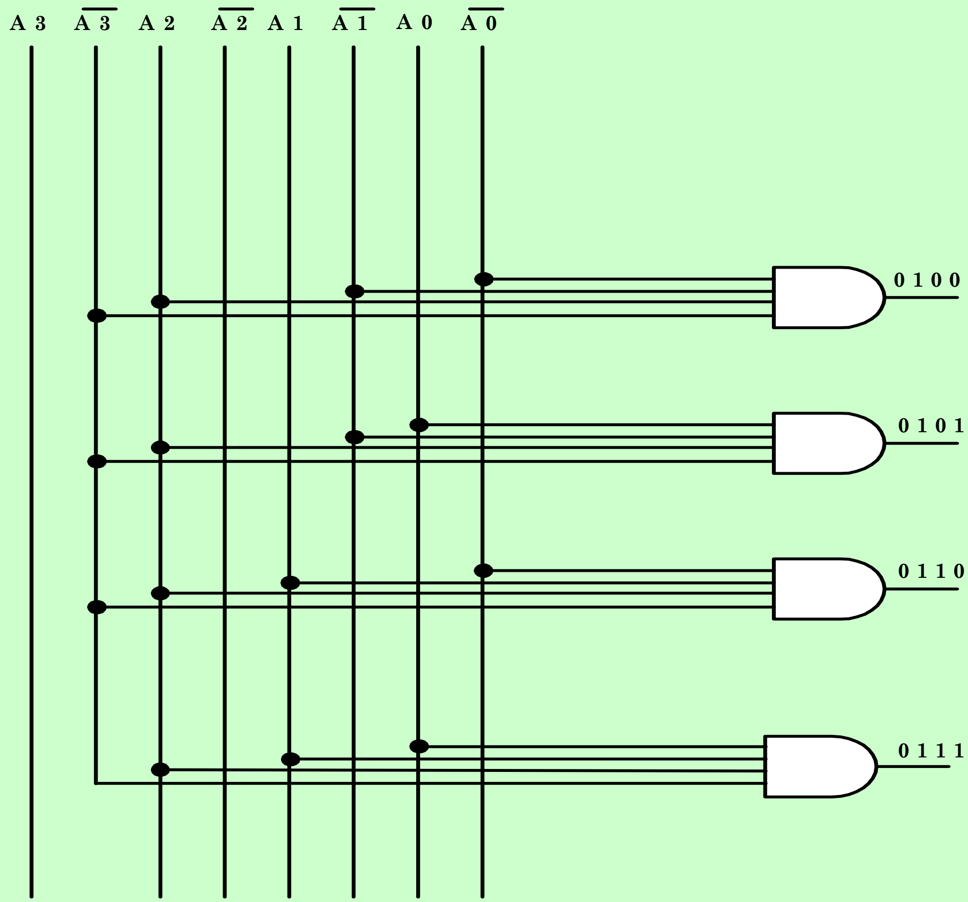
## 4 to 16 Decoder - Truth Table

| A3 | A2 | A1 | A0 | Value | Line |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0000 |
| 0 | 0 | 0 | 1 | 1 | 0001 |
| 0 | 0 | 1 | 0 | 2 | 0010 |
| 0 | 0 | 1 | 1 | 3 | 0011 |
| 0 | 1 | 0 | 0 | 4 | 0100 |
| 0 | 1 | 0 | 1 | 5 | 0101 |
| 0 | 1 | 1 | 0 | 6 | 0110 |
| 0 | 1 | 1 | 1 | 7 | 0111 |
| 1 | 0 | 0 | 0 | 8 | 1000 |
| 1 | 0 | 0 | 1 | 9 | 1001 |
| 1 | 0 | 1 | 0 | 10 | 1010 |
| 1 | 0 | 1 | 1 | 11 | 1011 |
| 1 | 1 | 0 | 0 | 12 | 1100 |
| 1 | 1 | 0 | 1 | 13 | 1101 |
| 1 | 1 | 1 | 0 | 14 | 1110 |
| 1 | 1 | 1 | 1 | 15 | 1111 |

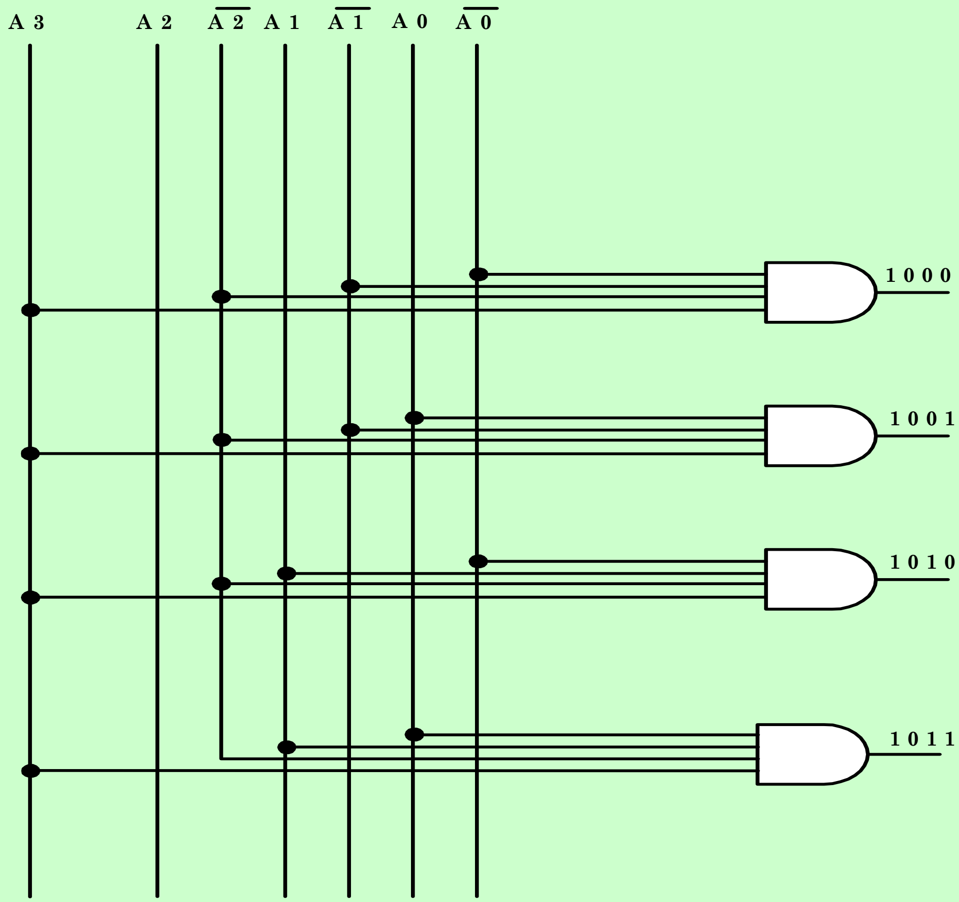
# 4 to 16 Decoder



## 4 to 16 Decoder - Page 2



## 4 to 16 Decoder - Page 3



# 4 to 16 Decoder - Page 4